DATA SHEET

SC28L92

3.3V–5.0V Dual Universal Asynchronous Receiver/Transmitter (DUART)

Product specification
Supersedes data of 1999 May 07
IC19 Data Handbook

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Philips
Semiconductors

PHILIPS

3.3V–5.0V Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

DESCRIPTION

The SC28L92 is a pin and function replacement for the SCC2692 and SC26C92 operating at 3.3 or 5 volts supply with added features and deeper FIFOs. Its configuration on power up is that of the SC26C92. Its differences from the 2692 are: 16 character receiver, 16 character transmit FIFOs, watch dog timer for each receiver, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (Neither the SC26C92 nor the SCC2692 is being discontinued.)

Pin programming will allow the device to operate with either the Motorola or Intel bus interface. The bit 3 of the MR0a register allows the device to operate in an 8 byte FIFO mode if strict compliance with the SC26C92 FIFO structure is required.

The Philips Semiconductors SC28L92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system with modem and DMA interface.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of 28 fixed baud rates; a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by 8 or 16 character FIFOs to minimize the potential of receiver overrun, transmitter underrun and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided via RTS/CTS signaling to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC28L92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC28L92 is available in two package versions: a 44-pin PLCC and 44-pin plastic quad flat pack (PQFP).

FEATURES

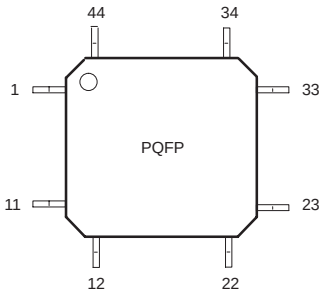
- Member of IMPACT family: 3.3 to 5.0 volt , –40°C to +85°C and 68K for 80xxx bus interface for all devices.
- Dual full-duplex independent asynchronous receiver/transmitters
- 16 character FIFOs for each receiver and transmitter
- Pin programming selects 68K or 80xxx bus interface
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 28 fixed rates: 50 to 230.4k baud
  - Other baud rates to MHz at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loop back
  - Remote loop back
  - Multi-drop mode (also called ‘wake-up’ or ‘9-bit’)
- Multi-function 7-bit input port (includes IACKN)
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
  - Change of state detectors for modem control
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
  - FIFO status for DMA interface
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate interrupt outputs that may be wire ORed.
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates:
  1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multi-drop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver time-out mode
- Single +3.3V or +5V power supply
- Powers up to emulate SC26C92

ORDERING INFORMATION

DESCRIPTION	INDUSTRIAL V_{CC} = +3.3 +5V ±10%, T_{amb} = –40 to +85°C	DRAWING NUMBER
44-Pin Plastic Leaded Chip Carrier (PLCC)	SC28L92A1A	SOT187–2
44-Pin Plastic Quad Flat Pack (PQFP)	SC28L92A1B	SOT307-2

PIN CONFIGURATION DIAGRAM

80XXX PIN CONFIGURATION



Pin	Function	Pin	Function	Pin	Function
1	A3	16	GND	31	x2
2	IP0	17	GND	32	RESET
3	WRN	18	INTRN	33	CEN
4	RDN	19	D6	34	IP2
5	RxDB	20	D4	35	IP6
6	TxDB	21	D2	36	IP5
7	OP1	22	D0	37	IP4
8	OP3	23	NC	38	V_{CC}
9	OP5	24	OP6	39	V_{CC}
10	OP7	25	OP4	40	A0
11	I/M	26	OP2	41	IP3
12	D1	27	OP0	42	A1
13	D3	28	TxDA	43	IP1
14	D5	29	RxDA	44	A2
15	D7	30	x1/clk		

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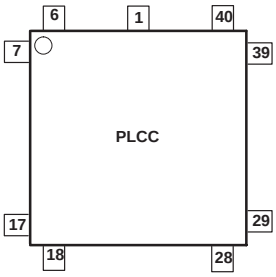

Pin	Function	Pin	Function	Pin	Function
1	NC	16	OP5	31	OP2
2	A0	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A1	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A2	21	D7	36	X1/CLK
7	A3	22	V_{SS}	37	X2
8	IP0	23	NC	38	RESET
9	WRN	24	INTRN	39	CEN
10	RDN	25	D6	40	IP2
11	RxDB	26	D4	41	IP6
12	I/M	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	V_{CC}
15	OP3	30	OP4		

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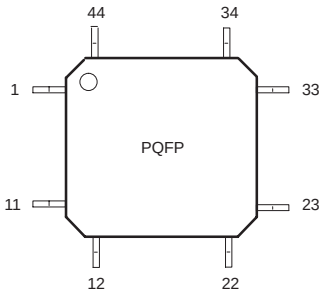
PIN CONFIGURATION DIAGRAM

68XXX PIN CONFIGURATION



Pin	Function	Pin	Function	Pin	Function
1	A3	16	GND	31	x2
2	IP0	17	GND	32	RESETN
3	R/WN	18	INTRN	33	CEN
4	DACKN	19	D6	34	IP2
5	RxDB	20	D4	35	IACKN
6	TxDB	21	D2	36	IP5
7	OP1	22	D0	37	IP4
8	OP3	23	NC	38	V_{CC}
9	OP5	24	OP6	39	V_{CC}
10	OP7	25	OP4	40	A0
11	I/M	26	OP2	41	IP3
12	D1	27	OP0	42	A1
13	D3	28	TxDA	43	IP1
14	D5	29	RxDA	44	A2
15	D7	30	x1/clk		

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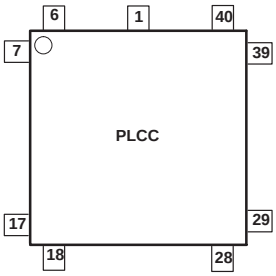


Pin	Function	Pin	Function	Pin	Function
1	NC	16	OP5	31	OP2
2	A0	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A1	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A2	21	D7	36	X1/CLK
7	A3	22	V_{SS}	37	X2
8	IP0	23	NC	38	RESETN
9	R/WN	24	INTRN	39	CEN
10	DACKN	25	D6	40	IP2
11	RxDB	26	D4	41	IACKN
12	I/M	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	V_{CC}
15	OP3	30	OP4		

SD00674

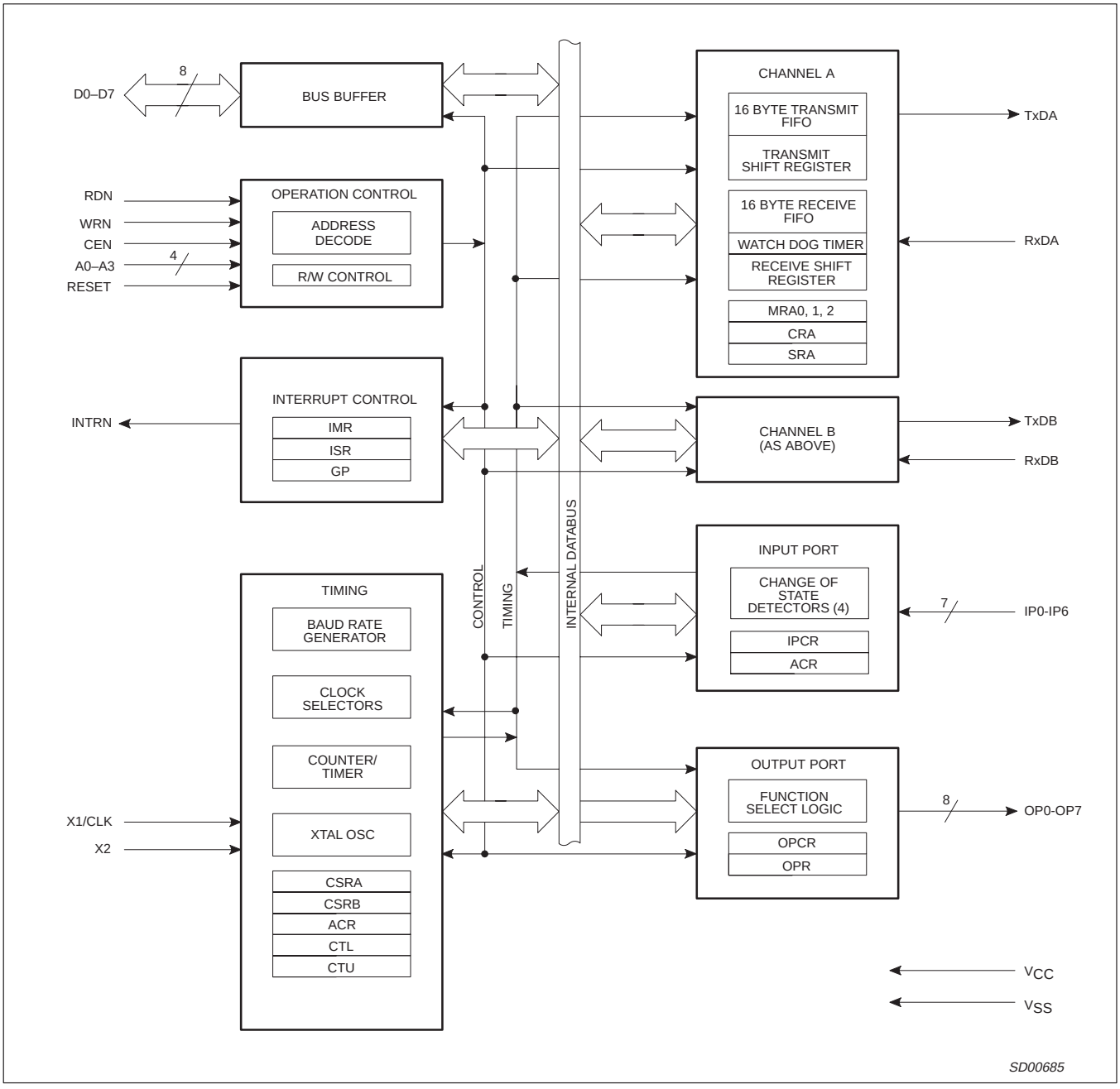


Figure 1. Block Diagram (80XXX mode)

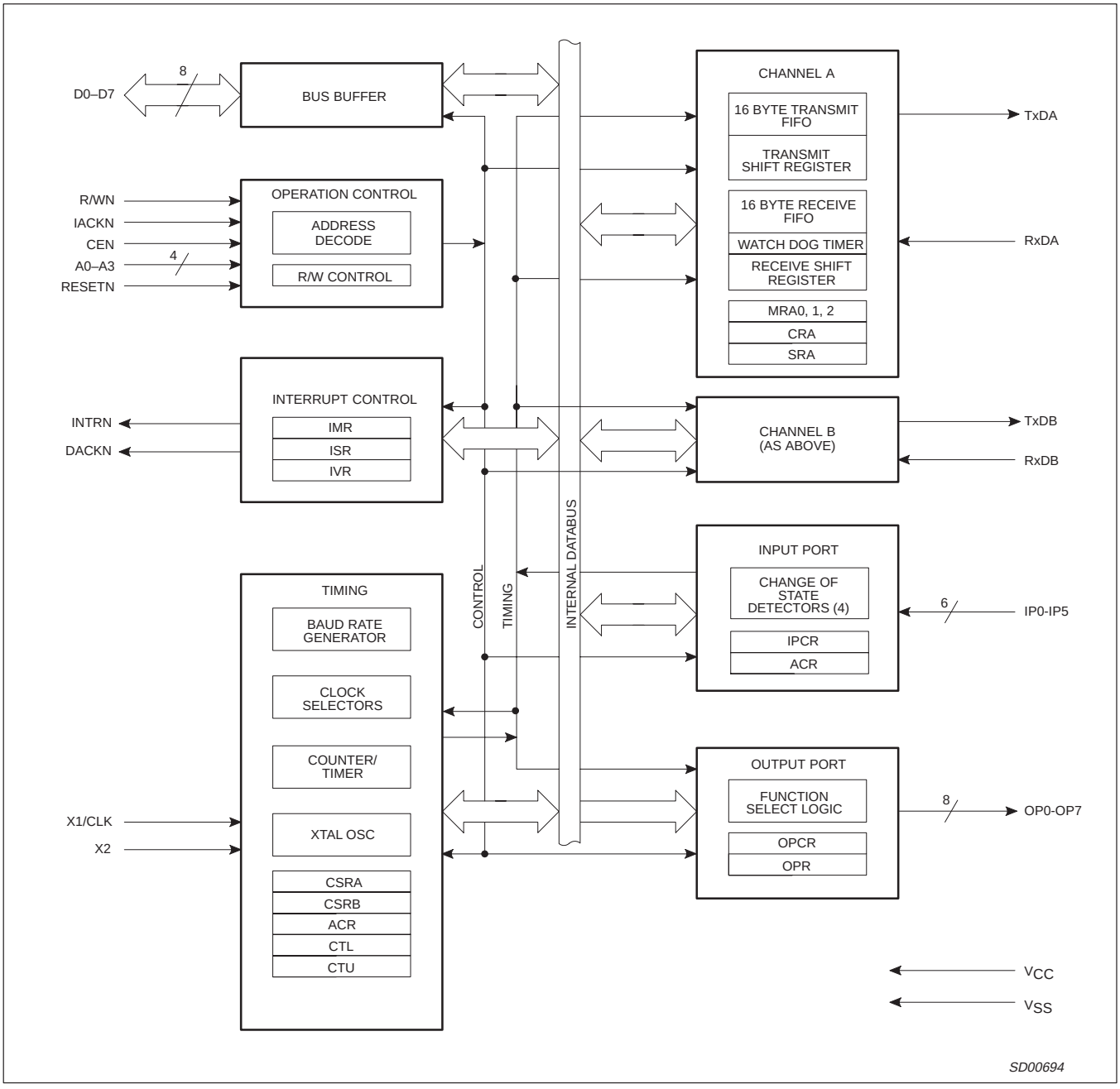


Figure 2. Block Diagram (68XXX mode)

PIN CONFIGURATION FOR 80XXX BUS INTERFACE (INTEL®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	**Bus Configuration**: When high or not connected configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	**Data Bus**: Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable**: Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
WRN	I	**Write Strobe**: When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe**: When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs**: Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset**: A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1. See Figure 4
INTRN	O	**Interrupt Request**: Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. This pin requires a pullup device.
X1/CLK	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 11).
X2	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 11). If X1/CLK is driven from an external source, this pin **must** be left open.
RxDA	I	**Channel A Receiver Serial Data Input**: The least significant bit is received first. “Mark” is High; “space” is Low.
RxDB	I	**Channel B Receiver Serial Data Input**: The least significant bit is received first. “Mark” is High; “space” is Low.
TxDA	O	**Channel A Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the “mark” condition when the transmitter is disabled, idle or when operating in local loop back mode. “Mark” is High; “space” is Low.
TxDB	O	**Channel B Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the ‘mark’ condition when the transmitter is disabled, idle, or when operating in local loop back mode. ‘Mark’ is High; ‘space’ is Low.
OP0	O	**Output 0**: General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1**: General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2**: General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3**: General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4**: General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR[1] output.
OP5	O	**Output 5**: General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	**Output 6**: General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	**Output 7**: General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	**Input 0**: General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	**Input 1**: General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	**Input 2**: General-purpose input or counter/timer external clock input.
IP3	I	**Input 3**: General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4**: General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5**: General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	I	**Input 6**: General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	Pwr	**Power Supply**: +3.3 or +5V supply input ±10%
GND	Pwr	**Ground**

PIN CONFIGURATION FOR 68XXX BUS INTERFACE (MOTOROLA®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	**Bus Configuration**: When low configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	**Data Bus**: Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable**: Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
R/WN	I	**Read/Write**: Input Signal. When CEN is low R/WN high input indicates a read cycle; when low indicates a write cycle.
IACKN	I	**Interrupt Acknowledge**: Active low input indicating an interrupt acknowledge cycle. Usually asserted by the CPU in response to an interrupt request. When asserted places the interrupt vector on the bus and asserts DACKN.
DACKN	O	**Data Transfer Acknowledge**: A3-State active -low output asserted in a write, read, or interrupt acknowledge cycle to indicate proper transfer of data between the CPU and the DUART.
A0–A3	I	**Address Inputs**: Select the DUART internal registers and ports for read/write operations.
RESETN	I	**Reset**: A low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1. See Figure 4
INTRN	O	**Interrupt Request**: Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. This pin requires a pullup.
X1/CLK	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 11).
X2	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 11). If X1/CLK is driven from an external source, this pin **must** be left open.
RxDA	I	**Channel A Receiver Serial Data Input**: The least significant bit is received first. “Mark” is High, “space” is Low.
RxDB	I	**Channel B Receiver Serial Data Input**: The least significant bit is received first. “Mark” is High, “space” is Low.
TxDA	O	**Channel A Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the “mark” condition when the transmitter is disabled, idle or when operating in local loop back mode. “Mark” is High; “space” is Low.
TxDB	O	**Channel B Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the ‘mark’ condition when the transmitter is disabled, idle, or when operating in local loop back mode. ‘Mark’ is High; ‘space’ is Low.
OP0	O	**Output 0**: General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1**: General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2**: General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3**: General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4**: General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR [1] output.
OP5	O	**Output 5**: General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	**Output 6**: General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	**Output 7**: General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	**Input 0**: General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	**Input 1**: General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	**Input 2**: General-purpose input or counter/timer external clock input.
IP3	I	**Input 3**: General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4**: General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5**: General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	Pwr	**Power Supply**: +3.3 or +5V supply input ±10%
GND	Pwr	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_{amb}	Operating ambient temperature range[2]	Note 4	°C
T_{stg}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	–0.5 to V_{CC} +0.5	V
P_D	Package power dissipation (PLCC44)	2.4	W
P_D	Package power dissipation (PQFP44)	1.78	W
	Derating factor above 25°C (PLCC44)	19	mW/°C
	Derating factor above 25°C (PQFP44)	14	mW/°C

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature and voltage range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

V_{CC} = 5V ± 10%, T_{amb} = –40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.4	1.5		V
V_{IH}	Input high voltage (X1/CLK)		0.8*V_{CC}	2.4		V
V_{OL}	Output low voltage	I_{OL} = 2.4mA		0.2	0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = -400µA	V_{CC} -0.5			V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	0.5	0.05	0.5	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	–130		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		130	µA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	–0.5	0.05	+0.5	µA
	Input port pins[5]	V_{IN} = 0 to V_{CC}	–8	0.05	+0.5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			0.5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–0.5			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	–0.5			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			0.5	µA
I_{CC}	Power supply current[6]					
	Operating mode	CMOS input levels		7	25	mA
	Power down mode	CMOS input levels		≤1	5	µA

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 3.0V with a transition time of 5ns maximum. For X1/CLK, this swing is between 0.4V and 0.8*V_{CC}. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 125pF, except open drain outputs. Test conditions for open drain outputs: C_L = 125pF, constant current source = 2.6mA.
5. Input port pins have active pull-up transistors that will source a typical 2µA from V_{CC} when the input pins are at V_{SS}. Input port pins at V_{CC} source 0.0µA.
6. All outputs are disconnected. Inputs are switching between CMOS levels of V_{CC} -0.2V and V_{SS} + 0.2V.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

V_{CC} = 3.3V ± 10%, T_{amb} = –40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage			0.65	0.2*V_{CC}	V
V_{IH}	Input high voltage		0.8*V_{CC}	1.7		V
V_{OL}	Output low voltage	I_{OL} = 2.4mA		0.2	0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = –400µA	V_{CC}–0.5	V_{CC}–0.2		V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	–0.5	0.05	+0.5	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	–80		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		80	µA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	–0.5	0.05	+0.5	µA
	Input port pins[5]	V_{IN} = 0 to V_{CC}	–8	0.5	+0.5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			0.5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–0.5			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	–0.5			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			0.5	µA
I_{CC}	Power supply current[6]					
	Operating mode	CMOS input levels			5	mA
	Power down mode	CMOS input levels		≤1	5.0	µA

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 3.0V with a transition time of 5ns maximum. For X1/CLK, this swing is between 0.4V and 0.8*V_{CC}. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 125pF, except open drain outputs. Test conditions for open drain outputs: C_L = 125pF, constant current source = 2.6mA.
5. Input port pins have active pull-up transistors that will source a typical 2µA from V_{CC} when the input pins are at V_{SS}. Input port pins at V_{CC} source 0.0µA.
6. All outputs are disconnected. Inputs are switching between CMOS levels of V_{CC} –0.2V and V_{SS}+0.2V.

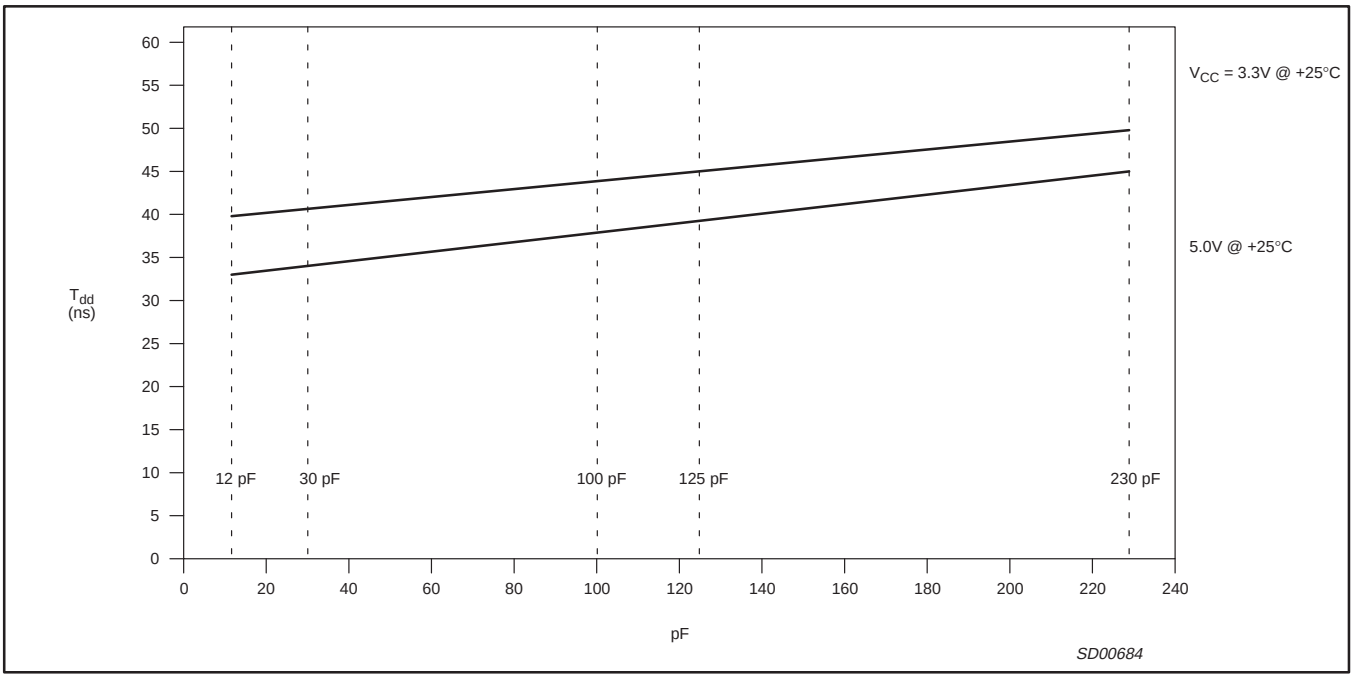
AC CHARACTERISTICS (5 VOLT) [1, 2, 3]

V_{CC} = 5.0V ± 10%, T_{amb} = –40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS[4]			UNIT
		Min	Typ	Max	
Reset Timing (See Figure 4)					
t_{RES}	Reset pulse width	100	18		ns
Bus Timing[5] (See Figure 5)					
t_{*AS}	A0–A3 setup time to RDN, WRN Low	10	6		ns
t_{*AH}	A0–A3 hold time from RDN, WRN low	20	12		ns
t_{*CS}	CEN setup time to RDN, WRN low	0			ns
t_{*CH}	CEN Hold time from RDN. WRN low	0			ns
t_{*RW}	WRN, RDN pulse width (Low time)	15	8		ns
t_{*DD}	Data valid after RDN low (125pF load. See Figure 3 for smaller loads.)		40	55	ns
t_{*DA}	RDN low to data bus active[6]	0			ns
t_{*DF}	Data bus floating after RDN or CEN high			20	ns
t_{*DI}	RDN or CEN high to data bus invalid[7]	0			ns
t_{*DS}	Data bus setup time before WRN or CEN high (write cycle)	25	17		ns
t_{*DH}	Data hold time after WRN high	0	–12		ns
t_{*RWD}	High time between read and/or write cycles[5, 7]	15	10		ns
Port Timing[5] (See Figure 9)					
t_{*PS}	Port in setup time before RDN low (Read IP ports cycle)	0	–20		ns
t_{*PH}	Port in hold time after RDN high	0	–20		ns
t_{*PD}	OP port valid after WRN or CEN high (OPR write cycle)		40	60	ns
Interrupt Timing (See Figure 10)					
t_{*IR}	INTRN (or OP3–OP7 when used as interrupts) negated from:				
	Read RxFIFO (RxRDY/FFULL interrupt)		40	60	ns
	Write TxFIFO (TxRDY interrupt)		40	60	ns
	Reset Command (delta break change interrupt)		40	60	ns
	Stop C/T command (Counter/timer interrupt		40	60	ns
	Read IPCR (delta input port change interrupt)		40	60	ns
	Write IMR (Clear of change interrupt mask bit(s))		40	60	ns
Clock Timing (See Figure 11)					
t_{*CLK}	X1/CLK high or low time	30	20		ns
f_{*CLK}	X1/CLK frequency[8]	0.1	3.686	8	MHz
f_{*CTC}	C/T Clk (IP2) high or low time (C/T external clock input)	30	10		ns
f_{*CTC}	C/T Clk (IP2) frequency[8]	0		8	MHz
t_{*RX}	RxC high or low time (16X)	30	10		ns
f_{*RX}	RxC Frequency (16X)	0		16	MHz
	RxC Frequency (1x)[8, 9]	0		1	MHz
t_{*TX}	TxC High or low time (16X)	30	10		ns
f_{*TX}	TxC frequency (16X)			16	MHz
	TxC frequency (1X)[8, 9]	0		1	MHz
Transmitter Timing, external clock (See Figure 12)					
t_{*TXD}	TxD output delay from TxC low (TxC input pin)		40	60	ns
t_{*TCS}	Output delay from TxC output pin low to TxD data output		6	30	ns

SYMBOL	PARAMETER	LIMITS[4]			UNIT
		Min	Typ	Max	
Receiver Timing, external clock (See Figure 13)					
t_{*RXS}	RxD data setup time to RxC high	50	40		ns
t_{*RXH}	RxD data hold time from RxC high	50	40		ns
68000 or Motorola bus timing (See Figures 6, 7, 8)[10]					
t_{DCR}	DACKN Low (read cycle) from X1 High[10]		15	20	ns
t_{DCW}	DACKN Low (write cycle) from X1 High		15	20	ns
t_{DAT}	DACKN High impedance from CEN or IACKN High		8	10	ns
t_{CSC}	CEN or IACKN setup time to X1 High for minimum DACKN cycle	10	8		ns

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4 V and 3.0 V with a transition time of 5 ns maximum. For X1/CLK this swing is between 0.4 V and 0.8*V_{CC}. All time measurements are referenced at input voltages of 0.8 V and 2.0 V and output voltages of 0.8 V and 2.0 V, as appropriate.
3. Test conditions for outputs: CL = 125 pF, except open drain outputs. Test conditions for open drain outputs: C_L = 125 pF, constant current source = 2.6mA.
4. Typical values are the average values at +25°C and 5V.
5. Timing is illustrated and referenced to the WRN and RDN Inputs. Also, CEN may be the “strobing” input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. Guaranteed by characterization of sample units.
7. If CEN is used as the “strobing” input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
8. Minimum frequencies are not tested but are guaranteed by design.
9. Clocks for 1X mode should maintain a 60/40 duty cycle or better.
10. Minimum DACKN time is $t_{DCR} = t_{DSC} + t_{DCR}$ + two positive edges of the X1 clock. For faster bus cycles, the 80XXX bus timing may be used while in the 68XXX mode. It is not necessary to wait for DACKN to insure the proper operation of the SC28C92. In all cases the data will be written to the SC28L92 on the falling edge of DACKN or the rise of CEN. The fall of CEN initializes the bus cycle. The rise of CEN ends the bus cycle. DACKN low or CEN high completes the write cycle.



NOTES:

Bus cycle times:

(80XXX mode): $t_{DD} + t_{RWD}$ = 70ns @ 5V, 40ns @ 3.3V + rise and fall time of control signals

(68XXX mode) = $t_{CSC} + t_{DAT}$ + 1 cycle of the X1 clock @ 5V + rise and fall time of control signals

Figure 3. Port Timing vs. Capacitive Loading at typical conditions

AC CHARACTERISTICS (3.3 VOLT) [1, 2, 3]

V_{CC} = 3.3V ± 10%, T_{amb} = –40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS[4]			UNIT
		Min	Typ	Max	
Reset Timing (See Figure 4)					
t_{RES}	Reset pulse width	100	20		ns
Bus Timing[5] (See Figure 5)					
t_{*AS}	A0–A3 setup time to RDN, WRN Low	10	6		ns
t_{*AH}	A0–A3 hold time from RDN, WRN low	25	16		ns
t_{*CS}	CEN setup time to RDN, WRN low	0			ns
t_{*CH}	CEN Hold time from RDN. WRN low	0			ns
t_{*RW}	WRN, RDN pulse width (Low time)	20	10		ns
t_{*DD}	Data valid after RDN low (125pF load. See Figure 3 for smaller loads.)		46	75	ns
t_{*DA}	RDN low to data bus active[6]	0			ns
t_{*DF}	Data bus floating after RDN or CEN high		15	20	ns
t_{*DI}	RDN or CEN high to data bus invalid[7]	0			ns
t_{*DS}	Data bus setup time before WRN or CEN high (write cycle)	25	20		ns
t_{*DH}	Data hold time after WRN high	0	–15		ns
t_{*RWD}	High time between read and/or write cycles[5, 7]	20	10		ns
Port Timing[5] (See Figure 9)					
t_{*PS}	Port in setup time before RDN low (Read IP ports cycle)	0	–20		ns
t_{*PH}	Port in hold time after RDN high	0	–20		ns
t_{*PD}	OP port valid after WRN or CEN high (OPR write cycle)		50	70	ns
Interrupt Timing (See Figure 10)					
t_{*IR}	INTRN (or OP3–OP7 when used as interrupts) negated from:				
	Read RxFIFO (RxRDY/FFULL interrupt)		40	60	ns
	Write TxFIFO (TxRDY interrupt)		40	60	ns
	Reset Command (delta break change interrupt)		40	60	ns
	Stop C/T command (Counter/timer interrupt		40	60	ns
	Read IPCR (delta input port change interrupt)		40	60	ns
	Write IMR (Clear of change interrupt mask bit(s))		40	60	ns
Clock Timing (See Figure 11)					
t_{*CLK}	X1/CLK high or low time	30	25		ns
f_{*CLK}	X1/CLK frequency[8]	0.1	3.686	8	MHz
f_{*CTC}	C/T Clk (IP2) high or low time (C/T external clock input)	30	15		ns
f_{*CTC}	C/T Clk (IP2) frequency[8]	0		8	MHz
t_{*RX}	RxC high or low time (16X)	30	10		ns
f_{*RX}	RxC Frequency (16X)	0		16	MHz
	RxC Frequency (1x)[8, 9]	0		1	MHz
t_{*TX}	TxC High or low time (16X)	30	15		ns
f_{*TX}	TxC frequency (16X)			16	MHz
	TxC frequency (1X)[8, 9]	0		1	MHz
Transmitter Timing, external clock (See Figure 12)					
t_{*TXD}	TxD output delay from TxC low (TxC input pin)		40	60	ns
t_{*TCS}	Output delay from TxC output pin low to TxD data output		8	30	ns

SYMBOL	PARAMETER	LIMITS[4]			UNIT
		Min	Typ	Max	
Receiver Timing, external clock (See Figure 13)					
t_{*RXS}	RxD data setup time to RxC high	50	10		ns
t_{*RXH}	RxD data hold time from RxC high	50	10		ns
68000 or Motorola bus timing (See Figures 6, 7, 8)[10]					
t_{DCR}	DACKN Low (read cycle) from X1 High[10]		18	25	ns
t_{DCW}	DACKN Low (write cycle) from X1 High		18	25	ns
t_{DAT}	DACKN High impedance from CEN or IACKN High		10	15	ns
t_{CSC}	CEN or IACKN setup time to X1 High for minimum DACKN cycle	15	10		ns

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4 V and 3.0 V with a transition time of 5 ns maximum. For X1/CLK this swing is between 0.4 V and 0.8*V_{CC}. All time measurements are referenced at input voltages of 0.8 V and 2.0 V and output voltages of 0.8 V and 2.0 V, as appropriate.
3. Test conditions for outputs: CL = 125 pF, except open drain outputs. Test conditions for open drain outputs: C_L = 125 pF, constant current source = 2.6mA.
4. Typical values are the average values at +25°C and 3.3V.
5. Timing is illustrated and referenced to the WRN and RDN Inputs. Also, CEN may be the “strobing” input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. Guaranteed by characterization of sample units.
7. If CEN is used as the “strobing” input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
8. Minimum frequencies are not tested but are guaranteed by design.
9. Clocks for 1X mode should maintain a 60/40 duty cycle or better.
10. Minimum DACKN time is $t_{DCR} = t_{DSC} + t_{DCR}$ + two positive edges of the X1 clock. For faster bus cycles, the 80XXX bus timing may be used while in the 68XXX mode. It is not necessary to wait for DACKN to insure the proper operation of the SC28C92. In all cases the data will be written to the SC28L92 on the falling edge of DACKN or the rise of CEN. The fall of CEN initializes the bus cycle. The rise of CEN ends the bus cycle. DACKN low or CEN high completes the write cycle.

Block Diagram
The SC28L92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer
The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control
The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus.

Interrupt Control
A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer. When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration. The OP pins may be used for DMA and modem control as well. (See output port notes).

FIFO Configuration
Each receiver and transmitter has a 16 byte FIFO. These FIFOs may be configured to operate at a fill capacity of either 8 or 16 bytes. This feature may be used if it is desired to operate the 28L92 in strict compliance with the 26C92. The 8 byte/16 byte mode is controlled by the MR0[3] bit. A 0 value for this bit sets the 8 bit mode (the default); a 1 sets the 16 byte mode.

The FIFO fill interrupt level automatically follow the programming of the MR0[3] bit. See Tables 3 and 4.

68XXX mode
When the I/M pin is connected to V_{CC} (ground), the operation of the SC28L92 switches to the bus interface compatible with the Motorola bus interfaces. Several of the pins change their function as follows:

Ip6 becomes IACKN input

RDN becomes DACKN

WRN becomes R/WN

The interrupt vector is enabled and the interrupt vector will be placed on the data bus when IACKN is asserted low. The interrupt vector register is located at address 0xC. The contents of this register are set to 0x0F on the application of RESETN.

The generation of DACKN uses two positive edges of the X1 clock as the DACKN delay from the falling edge of CEN. **If the CEN is withdrawn before two edges of the X1 clock occur, the generation of DACKN is terminated.** Systems not strictly requiring DACKN may use the 68XXX mode with the bus timing of the 80XXX mode greatly decreasing the bus cycle time.

TIMING CIRCUITS

Crystal Clock
The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 11. Nominal crystal rate is 3.6864 MHz. Rates up to 8 MHz may be used.

BRG
The baud rate generator operates from the oscillator or external clock input and is capable of generating 28 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a “1” gives additional baud rates of 57.6kB, 115.2kB and 230.4kB (531kHz with X1 at 8.5MHz). These will be in the 16X mode. A 3.6864 MHz crystal or external clock must be used to get the standard baud rates. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

Counter/Timer
The counter timer is a 16–bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the OP pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from 1 to 0. A register read address (see Table 1) is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop command. The value of D(7:0) is ignored. The START command always loads the contents of CTUR, CTLR to the counting registers. The STOP command always resets the ISR (3) bit in the interrupt status register.

Timer Mode
In the timer mode a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16–bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output will be equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode the ISR bit 3 (ISR[3]) will be set each time the counter/timer transitions from 1 to 0. (High to low)

This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command.

NOTE: Reading of the CTU and CTL registers in the timer mode is not meaningful. When the C/T is used to generate a baud rate and the C/T is selected through the CSR then the receivers and/or transmitter will be operating in the 16x mode. Calculation for the number 'n' to program the counter timer upper and lower registers is shown below. N=2 x 16 x Baud rate desired/(C/T Clock Frequency Often this division will result in a non–integer number; 26.3 for example. One can only program integer numbers to a digital divider. Therefore 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability of the asynchronous mode of operation.

Counter Mode

In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect. Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not stopped, a read of the C/T may result in changing data on the data bus.

Timeout Mode

The timeout mode uses the received data stream to control the counter. The time–out mode forces the C/T into the timer mode. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU will not be interrupted for the remaining characters in the RxFIFO.

By programming the C/T such that it would time out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time. NOTE: This is very similar to the watch dog time of MR0. The difference is in the programmability of the delay time and that the watchdog timer is restarted by either a receiver load to the RxFIFO or a system read from it.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. Only one receiver should use this mode at a time. However, if both are on, the timeout occurs after both receivers have been inactive for the timeout period. The start of the C/T will be on the logical or of the two receivers.

The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready Bit, ISR[3], will be set. If IMR [3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR [3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received. The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR CTUR Register descriptions.

Time Out Mode Caution

When operating in the special time out mode, it is possible to generate what appears to be a "false interrupt", i.e., an interrupt without a cause. This may result when a time–out interrupt occurs and then, BEFORE the interrupt is serviced, another character is received, i.e., the data stream has started again. (The interrupt latency is longer than the pause in the data stream.) In this case, when a new character has been receiver, the counter/timer will be restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR will show the "Counter Ready" bit not set. If nothing else is interrupting, this read of the ISR will return a x'00 character. This action may present the appearance of a spurious interrupt.

Communications Channels A and B

Each communications channel of the SC28L92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (Break Received, Framing and Parity Errors) are also FIFOed with each data character.

Input Port

The inputs to this unlatched 7-bit (6-bit for 68xxx mode) port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic, modem and DMA.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25–50 μs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port change of state detection circuitry uses a 38.4 kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25 μs (this assumes that the clock input is 3.6864 MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25 μs if the transition occurs "coincident with the first sample pulse". The 50 μs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25 μs later.

Output Port

The output ports are controlled from six places: the OPCR, OPR, MR, Command, SOPR and ROPR registers. The OPCR register

controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

These pins along with the IP pins and their change of state detectors are often used for modem and DMA control.

OPERATION

Transmitter

The SC28L92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC28L92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPT bits will be set in the status register. When a character is loaded to the transmit FIFO the TxEMPT bit will be reset. The TxEMPT will not set until: 1) the transmit FIFO is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit FIFO, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the TxFIFO while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the TxFIFO.

If the transmitter is disabled it continues operating until the character currently being transmitted and any characters in the TxFIFO, including parity and stop bits, have been transmitted. New data cannot be loaded to the TxFIFO when the transmitter is disabled.

When the transmitter is reset it stops sending data immediately.

The transmitter can be forced to send a break (a continuous low condition) by issuing a START BREAK command via the CR register. The break is terminated by a STOP BREAK command or a transmitter reset.

If CTS option is enabled (MR2[4] = 1), the CTS input at IP0 or IP1 must be Low in order for the character to be transmitted. The transmitter will check the state of the CTS input at the beginning of each character transmitted. If it is found to be High, the transmitter will delay the transmission of any following characters until the CTS has returned to the low state. CTS going high during the serialization of a character will not affect that character.

The transmitter can also control the RTSN outputs, OP0 or OP1 via MR2[5]. When this mode of operation is set, the meaning of the OP0 or OP1 signals will usually be 'end of message'. See description of the MR2[5] bit for more detail. This feature may be used to automatically "turn around" a transceiver in simplex systems.

Receiver

The SC28L92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive FIFO and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RxFIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR from the next byte to be read from the Rx FIFO. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RxFIFO and the received break bit in the SR is set to 1. The RxD input must return to high for two (2) clock edges of the X1 crystal clock for the receiver to recognize the end of the break condition and begin the search for a start bit.

This will usually require a high time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock.

Transmitter Reset and Disable

Note the difference between transmitter disable and reset. A transmitter reset stops transmitter action immediately, clears the transmitter FIFO and returns the idle state. A transmitter disable withdraws the transmitter interrupts but allows the transmitter to continue operation until all bytes in its FIFO and shift register have been transmitted including the final stop bits. It then returns to its idle state.

Receiver FIFO

The RxFIFO consists of a First-In-First-Out (FIFO) stack with a capacity of 8 or 16 characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all 8 or 16 stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RxFIFO outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated

status bits (see below) are ‘popped’ thus emptying a FIFO position for new data.

A disabled receiver with data in its FIFO may generate an interrupt (see “Receiver Status Bits”, below). Its status bits remain active and its watchdog, if enabled, will continue to operate.

Receiver Status Bits

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO. The overrun error, MR1(5), is not FIFOed.

Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the ‘character’ mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the ‘block’ mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last ‘reset error’ from the command register was issued. In either mode reading the SR does not affect the FIFO. The FIFO is ‘popped’ only when the RxFIFO is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted (set low) automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Receiver Reset and Disable

Receiver disable stops the receiver immediately—data being assembled in the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected.

A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers.

Watchdog

A ‘watchdog timer’ is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is to alert the control processor that characters are in the RxFIFO which have not been read. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the receiver shift register to the RxFIFO or a read of the RxFIFO is executed.

Receiver Time-out Mode

In addition to the watch dog timer described in the receiver section, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time out intervals.

The time-out mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the RxFIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

The time-out mode is enabled by writing the appropriate command to the command register. Writing an ‘Ax’ to CRA or CRB will invoke the time-out mode for that channel. Writing a ‘Cx’ to CRA or CRB will disable the time-out mode. The time-out mode should only be used by one channel at once, since it uses the C/T. If, however, the time-out mode is enabled from both receivers, the time-out will occur only when **both** receivers have stopped receiving data for the time-out period. CTU and CTL must be loaded with a value greater than the normal receive character period. The time-out mode disables the regular START/STOP Counter commands and puts the ca/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the ‘Set Time-out Mode On’ command, CRx = ‘Ax’, will also clear the counter ready bit and stop the counter until the next character is received.

Time Out Mode Caution

When operating in the special time out mode, it is possible to generate what appears to be a “false interrupt”, i.e., an interrupt without a cause. This may result when a time-out interrupt occurs and then, BEFORE the interrupt is serviced, another character is received, i.e., the data stream has started again. (The interrupt latency is longer than the pause in the data stream.) In this case, when a new character has been receiver, the counter/timer will be restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR will show the “Counter Ready” bit not set. If nothing else is interrupting, this read of the ISR will return a x’00 character.

Multi-drop Mode (9-bit or Wake-Up)

The DUART is equipped with a wake up mode for multi-drop applications. This mode is selected by programming bits

MR1A[4:3]or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY)only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while

MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the TxFIFO.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RxFIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RxFIFO. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has 3 mode registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register "Miscellaneous Commands". Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Philips Semiconductors UART software.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. SC28L92 register addressing READ (RDN = 0), WRITE (WRN = 0)

0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RxFIFOA)	Tx Holding Register A (TxFIFOA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Preset Register (CTPU)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Preset Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RxFIFOB)	Tx Holding Register B (TxFIFOB)
1	1	0	0	Interrupt vector (68K mode)	Interrupt vector (68K mode)
1	1	0	0	Misc. register (Intel mode), IVR Motorola mode	Misc. register (Intel mode), IVR Motorola mode
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command (SOPR)
1	1	1	1	Stop Counter Command	Reset output Port Bits Command (ROPR)

NOTE:
1. The three MR registers are accessed via the MR Pointer and Commands 0x1n and 0xBn (where n = represents receiver and transmitter enable bits)

The following named registers are the same for Channels A and B			
Mode Register	MRnA	MRnB	R/W
Status Register	SRA	SRB	R only
Clock Select	CSRA	CSRB	W only
Command Register	CRA	CRB	W only
Receiver FIFO	RxFIFOA	RxFIFOB	R only
Transmitter FIFO	TxFIFOA	TxFIFOB	W only

These are support functions for both Channels		
Input Port Change Register	IPCR	R
Auxiliary Control Register	ACR	W
Interrupt Status Register	ISR	R
Interrupt Mask Register	IMR	W
Counter Timer Upper Value	CTU	R
Counter Timer Lower Value	CTL	R
Counter Timer Preset Upper	CTPU	W
Counter Timer Preset Lower	CTPL	W
Input Port Register	IPR	R
Output Configuration Register	OPCR	W
Set Output Port	Bits	W
Reset Output Port	Bits	W
Interrupt vector or GP register	IVR/GP	R/W

Table 2. Condensed Register bit formats

MR0 – MODE REGISTER 0

Bit 7	BIT 6	BIT 5BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WATCHDOG	RxINT BIT 2	TxINT (1:0)	FIFO SIZE	BAUD RATE EXTENDED II	TEST 2	BAUD RATE EXTENDED 1

MR1 – MODE REGISTER 1

Bit 7	Bit 6	Bit 5	Bit 4:3	Bit 2	Bit 1:0
RxRTS Control	RxINT BIT 1	Error Mode	Parity Mode	Parity Type	Bits per Character

MR2 – MODE REGISTER 2

Bits 7:6	Bit 5	Bit 4	Bit 3:0
Channel Mode	TxRTS Control	CTSN Enable Tx	Stop Bit Length

CSR – CLOCK SELECT REGISTER

Bits 7:4	Bits 3:0
Receiver Clock,Select Code	Transmitter Clock select code,

CR –COMMAND REGISTER

Bits 7:4	Bit 3	Bit 2	Bit 1	Bit 0
Channel Command codes	Disable Tx	Enable Tx	Enable Tx	Enable Rx

SR – CHANNEL STATUS REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Received Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	RxFULL	RxRDY

IMR – INTERRUPT MASK REGISTER (ENABLES INTERRUPTS)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change Input Port	Change Break B	RxRDY B	TxRDTYB	Counter Ready	Change Break A	RxRDY A	TxRDY A

ISR – INTERRUPT STATUS REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change Input Port	Change Break B	RxRDY B	TxRDTYB	Counter Ready	Change Break A	RxRDY A	TxRDY A

CTPU – COUNTER TIMER PRESET REGISTERS, UPPER

Bits 7:0
8 MSB of the BRG Timer divisor.

CTPL – COUNTER TIMER PRESET REGISTER, LOWER

Bits 7:0
8 LSB of the BRG Timer divisor.

ACR – AUXILIARY CONTROL REGISTER AND CHANGE OF STATE CONTROL

Bit 7	Bit 6:4	Bit 3	Bit 2	Bit 1	Bit 0
Baud Group	Counter Timer mode and clock select	Enable IP3	Enable IP2	Enable IP1	Enable IP0

IPCR – INPUT PORT CHANGE REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delta IP3	Delta IP2	Delta IP1	Delta IP0	State of IP3	State of IP2	State of IP1	State of IP0

IPR – INPUT PORT REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
State of IP	State of IP 6	State of IP 5	State of IP 4	State of IP 3	State of IP 2	State of IP1	State of IP 0

SOPR – SET THE OUTPUT PORT BITS (OPR)

Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Set OP 7	Set OP 6	Set OP 5	Set OP 4	Set OP 3	Set OP 2	Set OP 1	Set OP 0

ROPR – RESET OUTPUT PORT BITS (OPR)

Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset OP 7	Reset OP 6	Reset OP 5	Reset OP 4	Reset OP 3	Reset OP 2	Reset OP 1	Reset OP 0

OPCR OUTPUT PORT CONFIGURATION REGISTER (NOTE OP1 AND OP0 ARE THE RTSN OUTPUT AND ARE CONTROLLED BY THE MR REGISTER)

Bit 7	BIT 6	BIT 5	BIT 4	BIT(3:2)	BIT(1:0)
Configure OP7	Configure OP6	Configure OP5	Configure OP4	Configure OP3	Configure OP2

REGISTER DESCRIPTIONS Mode Registers

MR0A Mode Register 0. MR0 is accessed by setting the MR pointer to 0 via the command register command B.

Addr	Bit 7	BIT 6	BITS 5:4	BIT 3	BIT 2	BIT 1	BIT 0
MR0A/ MR0B	Rx WATCHDOG	RxINT BIT 2	TxINT (1:0)	FIFO SIZE	BAUD RATE EXTENDED II	TEST 2	BAUD RATE EXTENDED 1
0x00 0x08	0 = Disable 1 = Enable	See Tables in MR0 description	See Table 4	0 = 8 byte FIFO 1 = 16 byte FIFO	0 = Normal 1 = Extend II	Set to 0	0 = Normal 1 = Extend

MR0[7]—This bit controls the receiver watch dog timer. 0 = disable, 1 = enable. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the RxFIFO that has not been read. This situation may occur when the byte count of the last part of a message is not large enough to generate an interrupt.

MR0[6]—Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the FIFO that generates the receiver interrupt.

MR0[6] MR1[6] Note that this control is split between MR0 and MR1. This is for backward compatibility to the SC2692 and SCN2681.

Table 3. Receiver FIFO interrupt fill level (MR0(3) = 0 (8 bytes)

MR0[6] MR1[6]	Interrupt Condition
00	1 or more bytes in FIFO (Rx RDY)
01	3 or more bytes in FIFO
10	6 or more bytes in FIFO
11	8 bytes in FIFO (Rx FULL)

Table 3a. Receiver FIFO interrupt fill level(MR0(3)=1 (16 bytes)

MR0[6] MR1[6]	Interrupt Condition
00	1 or more bytes in FIFO (Rx RDY)
01	8 or more bytes in FIFO
10	12 or more bytes in FIFO
11	16 bytes in FIFO (Rx FULL)

For the receiver these bits control the number of FIFO positions filled when the receiver will attempt to interrupt. After the reset the receiver FIFO is empty. The default setting of these bits cause the receiver to attempt to interrupt when it has one or more bytes in it.

MR0[5:4]—Tx interrupt fill level.

Table 4. Transmitter FIFO interrupt fill level MR0(3) = 0 (8 bytes)

MR0[5:4]	Interrupt Condition
00	8 bytes empty (Tx EMPTY)
01	4 or more bytes empty
10	6 or more bytes empty
11	1 or more bytes empty (Tx RDY)

Table 4a. Transmitter FIFO interrupt fill level MR0(3) = 1 (16 bytes)

MR0[5:4]	Interrupt Condition
00	16 bytes empty (Tx EMPTY)
01	8 or more bytes empty
10	12 or more bytes empty
11	1 or more bytes empty (Tx RDY)

For the transmitter these bits control the number of FIFO positions empty when the transmitter will attempt to interrupt. After the reset the transmit FIFO has 8 bytes empty. It will then attempt to interrupt as soon as the transmitter is enabled. The default setting of the MR0 bits (5:4) condition the transmitter to attempt to interrupt only when it is completely empty. As soon as one byte is loaded, it is no longer empty and hence will withdraw its interrupt request.

MR0[3]—Selects the FIFO depth at 8 or 16 bytes. See Tables 3 and 4

MR0[2:0]—These bits are used to select one of the six baud rate groups.

See Table 5 for the group organization.

000 Normal mode
001 Extended mode I
100 Extended mode II

Other combinations of MR2[2:0] should not be used

Note: MR0[3:0] are not used in channel B and should be set to 0.

MR1A Mode Register 1

Addr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR1A/ MR1B	Rx CONTROLS RTS	RxINT BIT 1	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHARACTER	
0x00 0x08	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multi-drop Mode		0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8	

NOTE:
In block error mode, block error conditions must be cleared by using the error reset command (command 4x) or a receiver reset.

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CR command 1. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7]—Channel A Receiver Request-to-Send Control (Flow Control)
This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. Proper automatic operation of flow control requires OPR[0] (channel A) or OPR[1] (channel B) to be set to logical 1.

MR1A[7] = 1 causes RTSAN to be negated (OP0 is driven to a '1' [V_{CC}]) upon receipt of a valid start bit if the Channel A FIFO is full. This is the beginning of the reception of the ninth byte. If the FIFO is not read before the start of the tenth or 17th byte, an overrun condition will occur and the tenth or 17th or 17th byte will be lost. However, the bit in OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1[6]—Bit 1 of the receiver interrupt control. See description under MR0[6].

MR1A[5]—Channel A Error Mode Select
This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3|—Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multi-drop mode described in the Operation section.

MR1A[2]—Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no

parity' mode is programmed. In the special multi-drop mode it selects the polarity of the A/D bit.

MR1A[1:0]—Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A—Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2 MODE REGISTER 2

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR2A/B	CHANNEL MODE		Tx CONTROLS RTS	CTS ENABLE Tx	STOP BIT LENGTH NOTE: Add 0.5 to binary codes 0–7 for 5 bit character lengths.			
0x00 0x08	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop		0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
Add 0.5 to values shown for 0–7 if channel is programmed for 5 bits/char.

MR2A[7:6]—Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently.

MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

MR2A[7:6] = 10 selects local loop back diagnostic mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

MR2A[7:6] = 11 selects remote loop back diagnostic mode. In this mode:

1. Received data is reclocked and retransmitted on the TxDA out-put.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of auto echo or remote loop back modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in auto echo by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in auto echo mode until the entire stop has been re-transmitted.

MR2A[5]—Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the TxFIFO, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled.

This feature can be used to automatically terminate the transmission of a message as follows (“line turnaround”):

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A TxFIFO.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4]—Channel A Clear-to-Send Control

If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0]—Channel A Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a ‘mark’ condition at the center of the stop bit position (one half-bit time after the last data bit, or after the parity bit if enabled is sampled).

If an external 1X clock is used for the transmitter, then MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR0B—Channel B Mode Register 0

MR0B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR0 by RESET or by a ‘set pointer’ command applied via CRB. After reading or writing MR0B, the pointer will point to MR1B.

The bit definitions for this register are identical to MR0A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs. MR0B[3:0] are reserved.

MR1B—Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a ‘set pointer’ command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B—Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSR CLOCK SELECT REGISTER

Addr	CSR (7:4)	CSR (3:0)
CSRA/B	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
0x01 0x09	See Text and table 5	See Text and table 5

Table 5. Baud rate (base on a 3.6864MHz crystal clock)

	MR0[0] = 0 (Normal Mode)		MR0[0] = 1 (Extended Mode I)		MR0[2] = 1 (Extended Mode II)	
CSRA[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	300	450	4,800	7,200
0001	110	110	110	110	880	880
0010	134.5	134.5	134.5	134.5	1,076	1,076
0011	200	150	1200	900	19.2K	14.4K
0100	300	300	1800	1800	28.8K	28.8K
0101	600	600	3600	3600	57.6K	57.6K
0110	1,200	1,200	7200	7,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1001	4,800	4,800	28.8K	28.8K	4,800	4,800
1010	7,200	1,800	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	57.6K	57.6K	9,600	9,600
1100	38.4K	19.2K	230.4K	115.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer	Timer	Timer
1110	IP4–16X	IP4–16X	IP4–16X	IP4–16X	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X	IP4–1X	IP4–1X	IP4–1X	IP4–1X

NOTE:
The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRA[3:0]—Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 5, except as follows:

CSRA[3:0]	
1110	1111
IP3–16X	IP3–1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

CSRB—Channel B Clock Select Register

CSRB[7:4]—Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 5, except as follows:

CSRB[7:4]	
1110	1111
IP6–1X	IP6–16X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0]—Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 5, except as follows:

CSRB[3:0]	
1110	1111
IP5–1X	IP5–16X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

Table 6. Bit rate generator characteristics

Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (KHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE:
Duty cycle of 16X clock is 50% ±1%

CRA—Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CR COMMAND REGISTER

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA/B	MISCELLANEOUS COMMANDS				Disable Tx	Enable Tx	Disable Rx	Enable Rx
0x02 0x0A	See Text of Channel Command Register				1 = Yes 0 = No	1 = Yes 0 = No	1 = Yes 0 = No	1 = Yes 0 = No

NOTES:
Access to the miscellaneous commands should be separated by 3 X1 clock edges. A disabled transmitter cannot be loaded.

CRA[7:4]—Miscellaneous Commands
Execution of the commands in the upper four bits of this register must be separated by 3 X1 clock edges. Other reads or writes (including writes tot he lower four bits) may be inserted to achieve this separation.

CRA[7:4]—Commands

0000 No command.

0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero

0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High)

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset. (See also Watchdog timer description in the receiver section.)

1011 Set MR pointer to '0'

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued to force a reset of the ISR(3) bit

1101 Not used.

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only. For maximum power reduction input pins should be at V_{SS} or V_{DD}.

CRA[3]—Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2]—Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY and TxEMT status bits will be asserted if the transmitter is idle.

CRA[1]—Disable Channel A Receiver
This command terminates operation of the receiver immediately—a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multi-drop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0]—Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB—Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of commands "Ex" and "Fx" which are used for power down mode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SR STATUS REGISTER Channel A Status Register

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SRA/B	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
0x01 0x09	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO. In block error mode, the error-reset command (command 4x or receiver reset)must used to clear block error conditions

SRA[7]—Channel A Received Break This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time two successive edges of the internal or external 1X clock. **This will usually require a high time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock**.

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

This bit is reset by command 4 (0100) written to the command register or by receiver reset.

SRA[6]—Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected (not a logical 1) when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5]—Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multi-drop mode the parity error bit stores the receive A/D (Address/Data) bit.

SRA[4]—Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3]—Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter under runs, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the under run condition.

SRA[2]—Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the transmit FIFO is not full and ready to be loaded with another character. This bit is cleared when the transmit FIFO is loaded by the CPU and there are (after this load) no more empty locations in the FIFO. It is set when a character is transferred to the transmit shift register. TxRDYA is reset when the transmitter is disabled and is set when the transmitter is first enabled. Characters loaded to the TxFIFO while this bit is 0 will be lost. This bit has different meaning from ISR[0].

SRA[1]—Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight (or 16) FIFO positions are occupied. It is reset when the CPU reads the receive FIFO. If a character is waiting in the receive shift register because the FIFO is full, FFULLA will not be reset when the CPU reads the receive FIFO. This bit has different meaning from ISR1 when MR1 6 is programmed to a '1'.

SRA[0]—Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset

when the CPU reads the receive FIFO, only if (after this read) there are no more characters in the FIFO – the Rx FIFO becomes empty.

SRB—Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR—Output Port Configuration Register

OPCR OUTPUT PORT CONFIGURATION REGISTER

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OPCR	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0x0D	0 = OPR[7] 1 = TxRDY B	0 = OPR[6] 1 = TxRDY A	0 = OPR[5] 1 = RxRDY/FFULL B	0 = OPR[4] 1 = RxRDY/FFULL A	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)		00 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)	

OPCR[7]—OP7 Output Select
This bit programs the OP7 output to provide one of the following:

0 The complement of OPR[7].

1 The Channel B transmitter interrupt output which is the complement of ISR[4]. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6]—OP6 Output Select
This bit programs the OP6 output to provide one of the following:

0 The complement of OPR[6].

1 The Channel A transmitter interrupt output which is the complement of ISR[0]. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5]—OP5 Output Select
This bit programs the OP5 output to provide one of the following:

0 The complement of OPR[5].

1 The Channel B receiver interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4]—OP4 Output Select
This field programs the OP4 output to provide one of the following:

0 The complement of OPR[4].

1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2]—OP3 Output Select
This bit programs the OP3 output to provide one of the following:

00 The complement of OPR[3].

01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.

10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.

11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0]—OP2 Output Select

This field programs the OP2 output to provide one of the following:

00 The complement of OPR[2].

01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.

10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.

11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

SOPR—Set the Output Port Bits (OPR)

SOPR[7:0]—Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect. This allows software to set individual bits with our keeping a copy of the OPR bit configuration.

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SOPR	**OP 7**	**OP 6**	**OP 5**	**OP 4**	**OP 3**	**OP 2**	**OP 1**	**OP 0**
0x0E	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change

ROPR—Reset Output Port Bits (OPR)

ROPR[7:0]—Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect. This allows software to reset individual bits with our keeping a copy of the OPR bit configuration.

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ROPR	**OP 7**	**OP 6**	**OP 5**	**OP 4**	**OP 3**	**OP 2**	**OP 1**	**OP 0**
0x0F	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change

OPR Output Port Register

The output pins (OP pins) drive the compliment of the data in this register as controlled by SOPR and ROPR.

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N/A	**OP 7**	**OP 6**	**OP 5**	**OP 4**	**OP 3**	**OP 2**	**OP 1**	**OP 0**
N/A	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low

ACR Auxiliary Control Register

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACR	BRG SET Select	Counter Timer Mode Mode and clock sour select			Delta IP3 int enable	Delta IP3 int enable	Delta IP3 int enable	Delta IP3 int enable
0x04	0 = set 1 1 = set 2	See table 7			0 = off 1 = enabled	0 = off 1 = enabled	0 = off 1 = enabled	0 = off 1 = enabled

ACR—Auxiliary Control Register

ACR[7]—Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG (see Table 5).

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 6.

ACR[6:4]—Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 7

ACR [3:0]—IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR [7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR [7], which results in the generation of an interrupt output if IMR [7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR [7].
NOTE:
The timer mode generates a square wave

Table 7. ACR 6:4 field definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA - 1X clock of Channel A transmitter
010	Counter	TxCB - 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

IPCR INPUT PORT CHANGE REGISTER

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IPCR	Delta IP3	Delta IP3	Delta IP3	Delta IP3	IP 3	IP 2	IP 1	IP 0
0x04	0 = no change 1 = change	0 = no change 1 = change	0 = no change 1 = change	0 = no change 1 = change	0 = low 1 = High	0 = low 1 = High	0 = low 1 = High	0 = low 1 = High

IPCR [7:4]—IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR [7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR [3:0]—IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR—Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR - the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to H'00' when the DUART is reset.

ISR INTERRUPT STATUS REGISTER

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR	INPUT PORT CHANGE	DELTA Break B	RxRDY/ FFULL B	TxRDY B	Counter Ready	Delta Break A	RxRDY/ FFULL A	TxRDY A
0x05	0 = not active 1 = active	0 = not active 1 = active	0 = not active 1 = active	0 = not active 1 = active	0 = not active 1 = active	0 = not active 1 = active	0 = not active 1 = active	0 = not active 1 = active

ISR[7]—Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6]—Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5]—RxB Interrupt
This bit indicates that the channel B receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[4]—TxB Interrupt
This bit indicates that the channel B transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

ISR[3]—Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2]—Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1]—RxA Interrupt
This bit indicates that the channel A receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[0]—TxA Interrupt
This bit indicates that the channel A transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

IMR—Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

IMR INTERRUPT MASK REGISTER

Addr	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR	INPUT PORT CHANGE	Delta Break B	RxRDY/ FFULL B	TxRDY B	Counter Ready	Delta Break A	RxRDY/ FFULL A	TxRDY A
0x05	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled

IVR/GP – Interrupt Vector Register (68XXX mode) or General Purpose register (80XXX mode)

IVR/GP	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0C	Interrupt Vector Register (68XXX mode) or General Purpose register (80XXX mode)							

This register stores the Interrupt Vector. It is initialized to 0x0F on hardware reset and is usually changed from this value during initialization of the SC26L92. The contents of this register will be placed on the data bus when IACKN is asserted low or a read of address 0xC is performed.

When not operating in the 68XXX mode, this register may be used as a general purpose one byte storage register. A convenient use could be to store a “shadow” of the contents of another SC28L92 register (IMR, for example).

CTPU and CTPL – Counter/Timer Registers

CTPU COUNTER TIMER PRESET UPPER

CTPU	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x06	The lower eight (8) bits for the 16 bit counter timer preset register							

CTPL COUNTER -TIMER PRESET LOW

CTPL	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x07	The Upper eight (8) bits for the 16 bit counter timer preset register							

The CTPU and CTPL hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTPU/CTPL registers is H‘0002’. Note that these registers are write-only and cannot be read by the CPU.

In the timer mode, the C/T generates a square wave whose period is twice the value (in C/T clock periods) of the CTPU and CTPL. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTPU and CTPL for a particular 1X data clock is shown below.

n = (C/T Clock Frequency) divided by (2 x 16 x Baud rate desired)

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

The C/T will not be running until it receives an initial ‘Start Counter’ command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTPU and CTPL. If the value in CTPU and CTPL is changed, the current half-period will not be affected, but subsequent half periods will be affected.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H’F’). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output. In the counter mode, the value C/T loaded into CTPU and CTPL by the CPU is counted down to 0.. Counting begins upon receipt of a start counter command. Upon reaching terminal count 0x0000, the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTPU and CTPL at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTPU and CTPL.

When the C/T clock divided by 16 is selected, the maximum divisor becomes 1,048,575.

Output Port Notes

The output ports are controlled from four places: the OPCR register,the OPR register, the MR registers and the command register (except the 2681 and 68681) The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register.

The content of the OPR register is controlled by the “Set Output Port Bits Command” and the “Reset Output Bits Command”. These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the “Set Output Port Bits” command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the “Reset Output Ports Bits” command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB. RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is,

thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the ninth or 17th character is sensed. Transmission then stops with nine or 17 valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter. MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be.

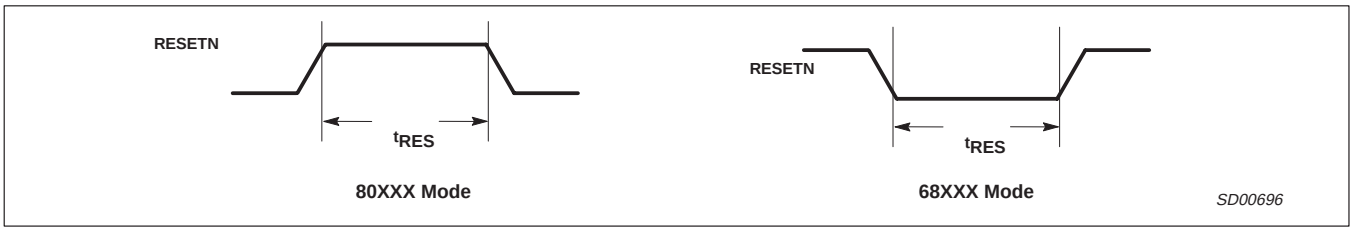


Figure 4. Reset Timing

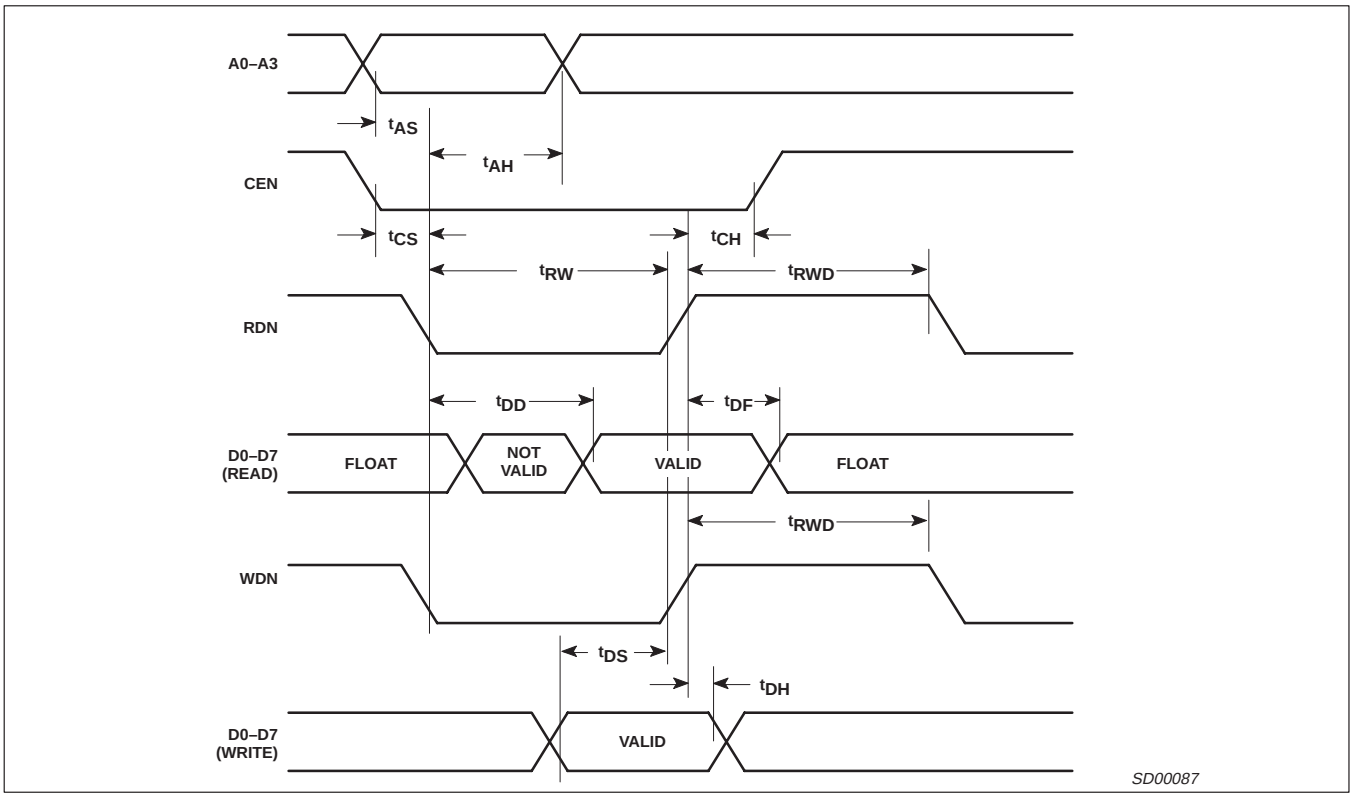
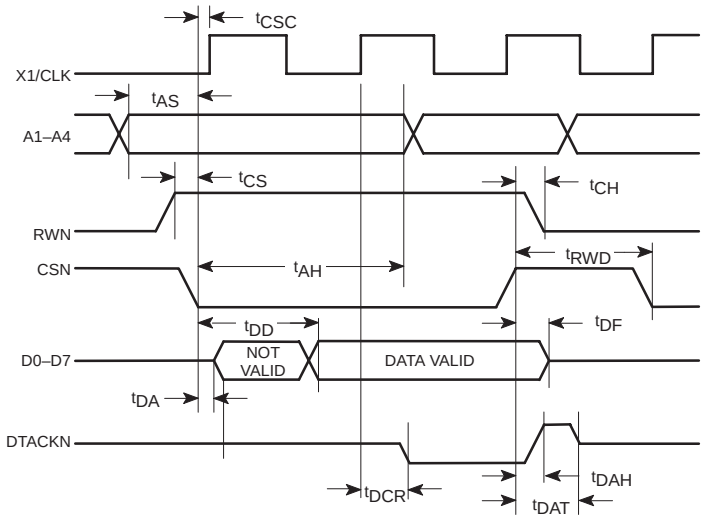


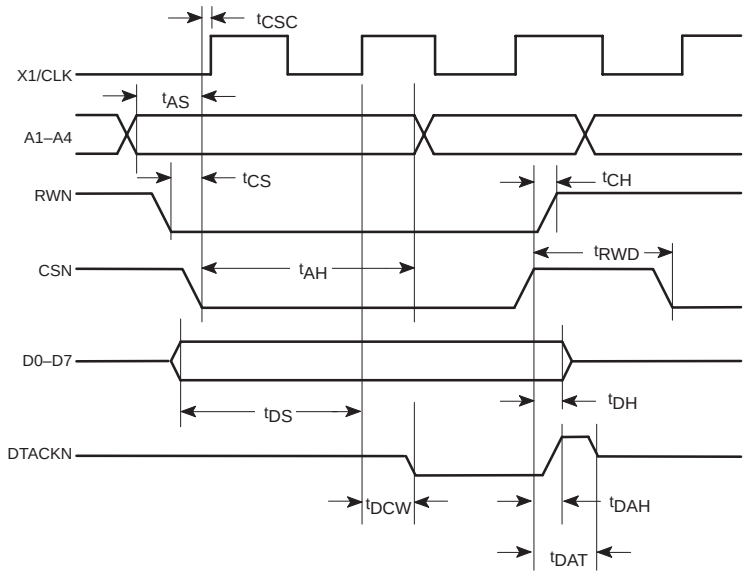
Figure 5. Bus Timing (80XXX mode)



NOTE: DACKN low requires two rising edges of X1 clock after CSN is low.

SD00687

Figure 6. Bus Timing (Read Cycle) (68XXX mode)



NOTE: DACKN low requires two rising edges of X1 clock after CSN is low.

SD00688

Figure 7. Bus Timing (Write Cycle) (68XXX mode)

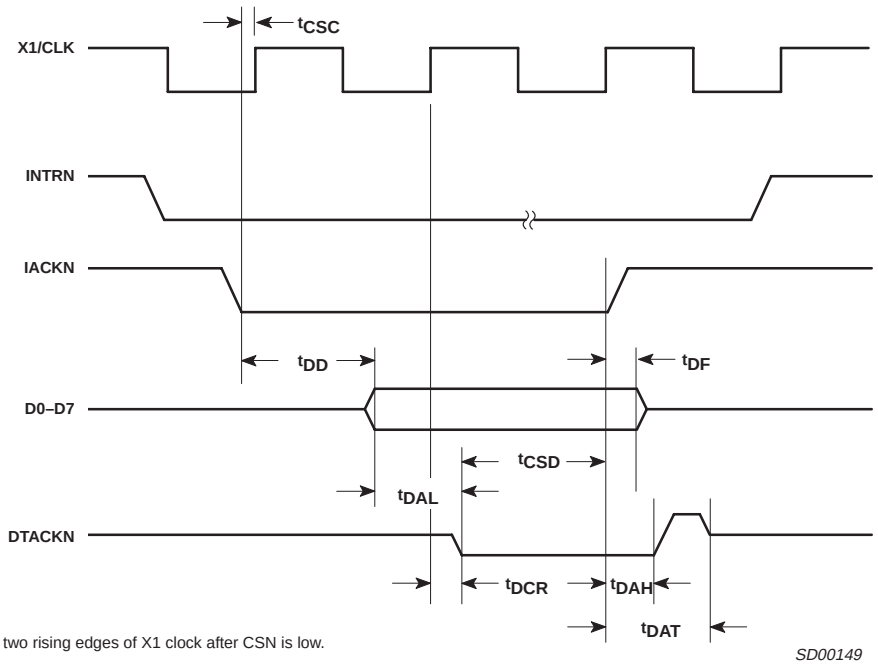


Figure 8. Interrupt Cycle Timing (68XXX mode)

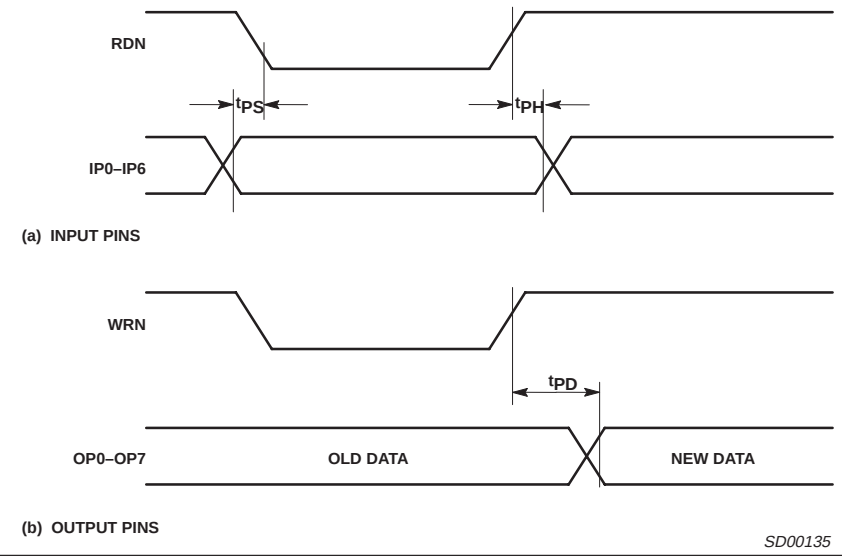
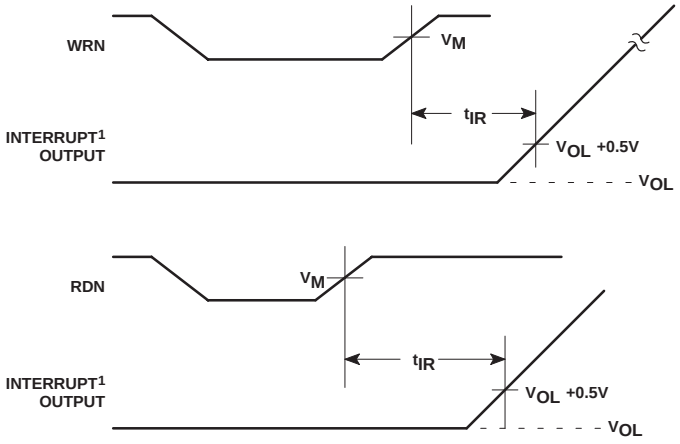


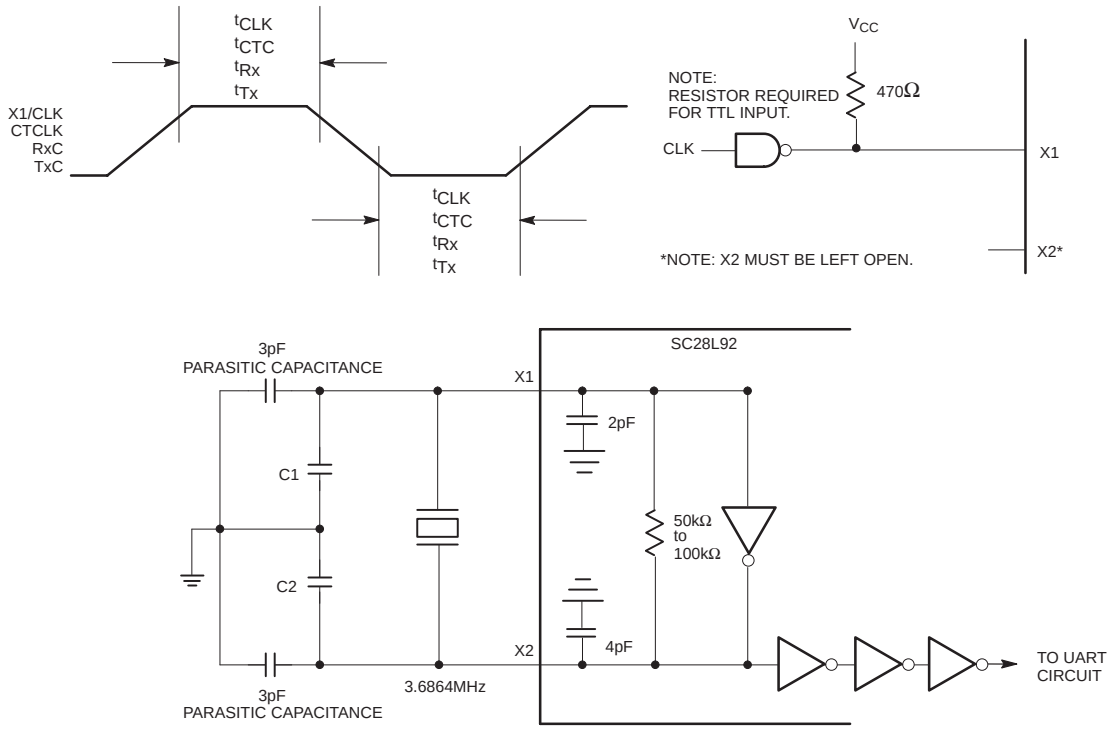
Figure 9. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

SD00136

Figure 10. Interrupt Timing (80xxx mode)



C1 = C2 ~ 24pF FOR C_L = 20pF
C1 and C2 should be chosen according to the crystal manufacturer's specification.
C1 and C2 values will include any parasitic capacitance of the wiring and X1 X2 pins.
Gain at 3.6864MHz: 9 to 13 dB
Package capacitance approximately 4pF.

SD00695

Figure 11. Clock Timing

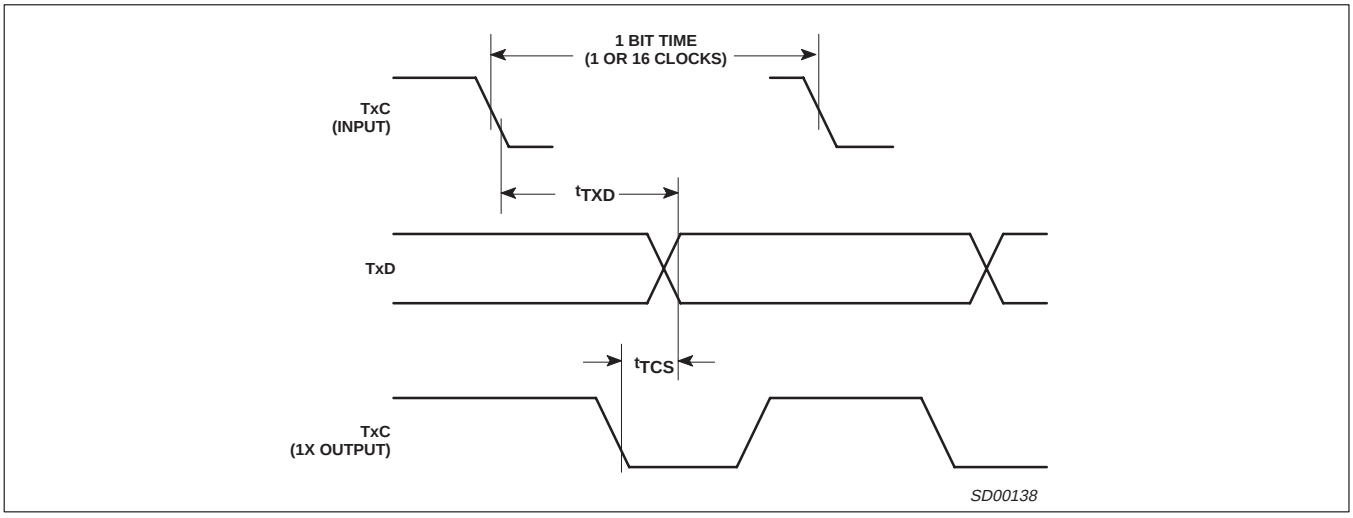


Figure 12. Transmitter External Clocks

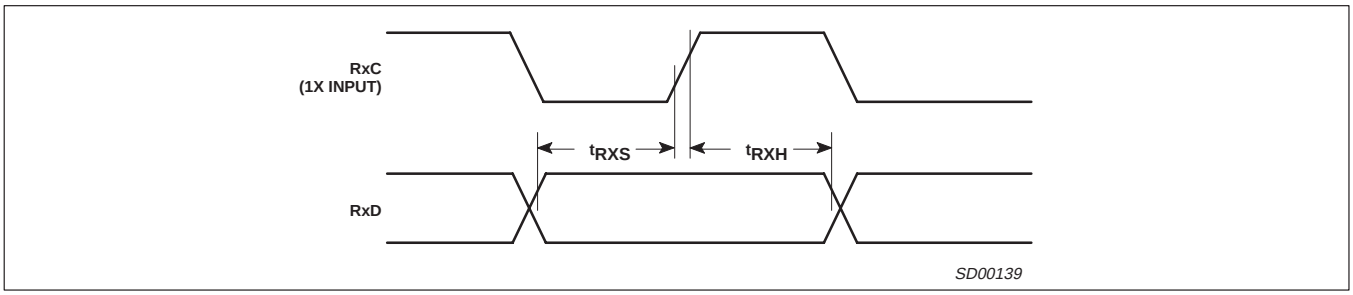


Figure 13. Receiver External Clock

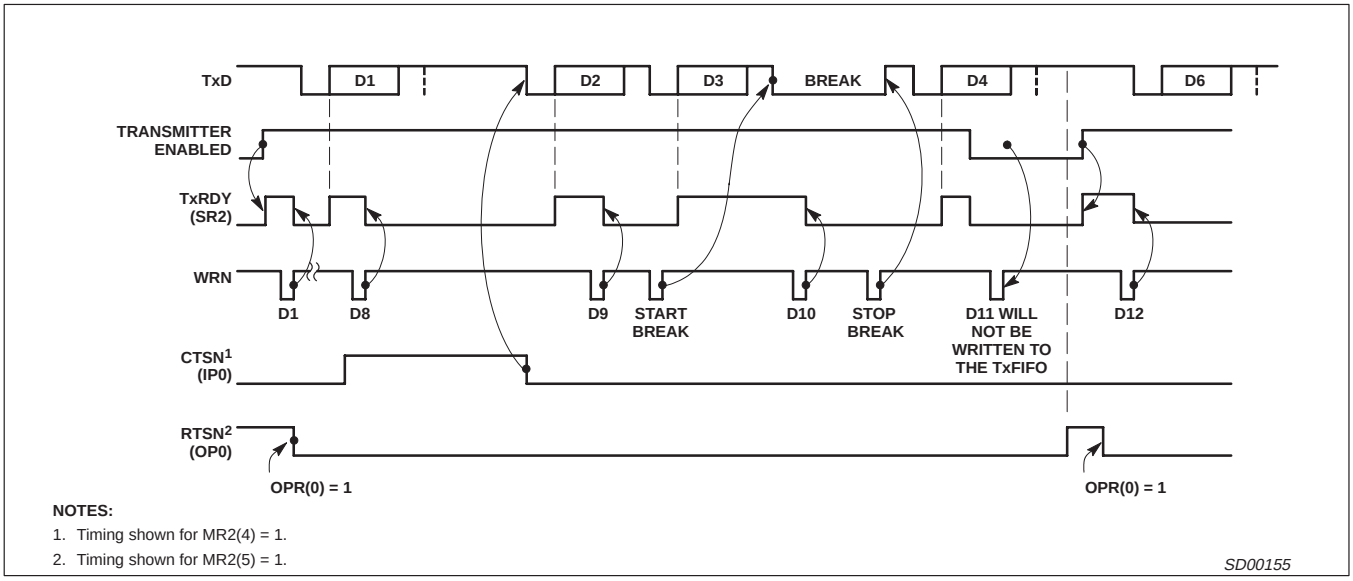


Figure 14. Transmitter Timing

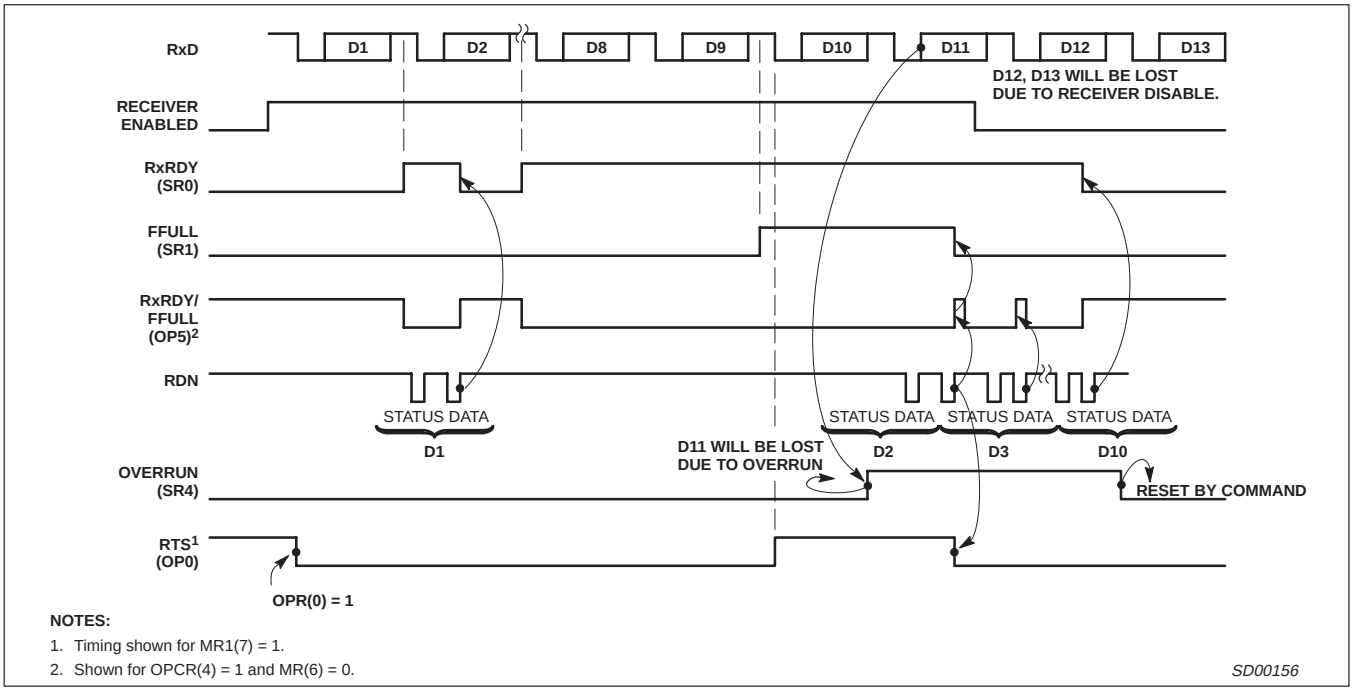


Figure 15. Receiver Timing

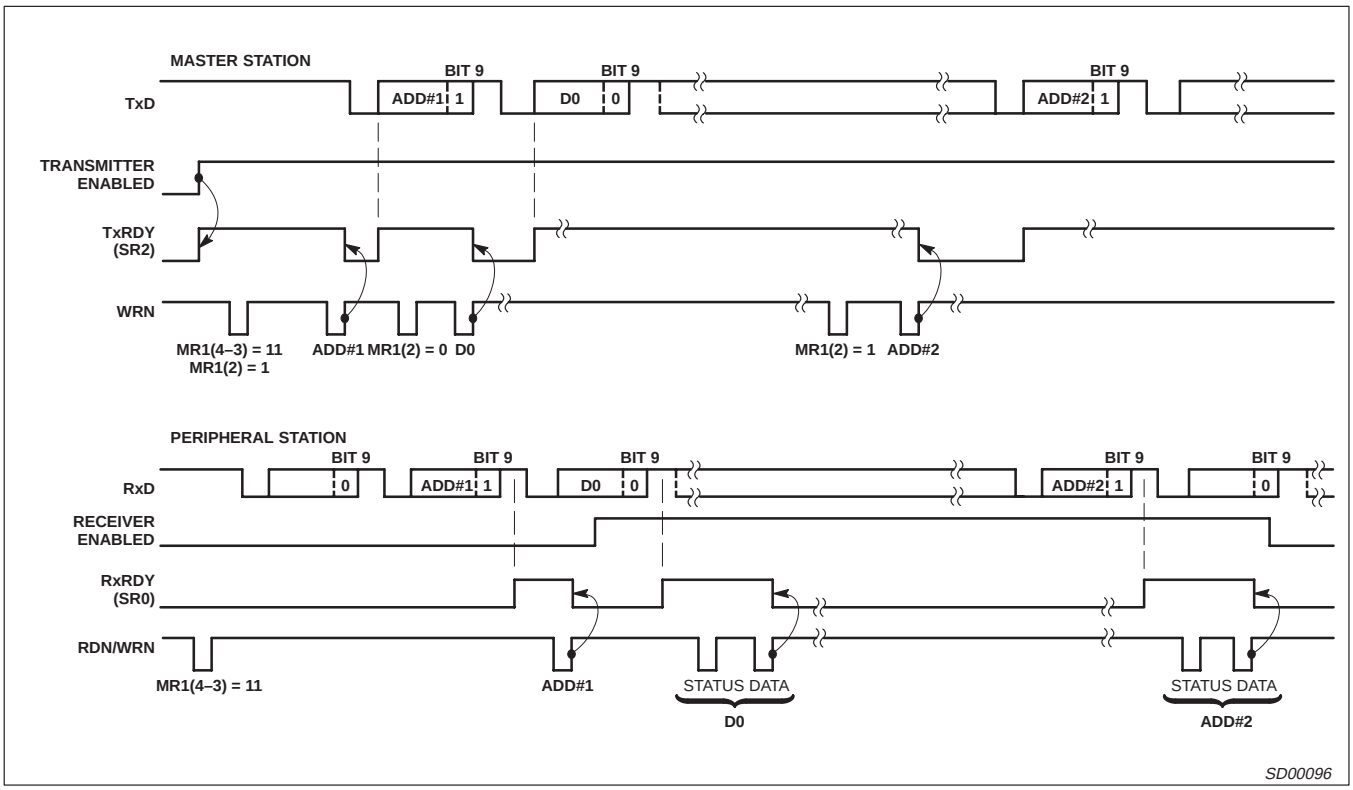


Figure 16. Wake-Up Mode

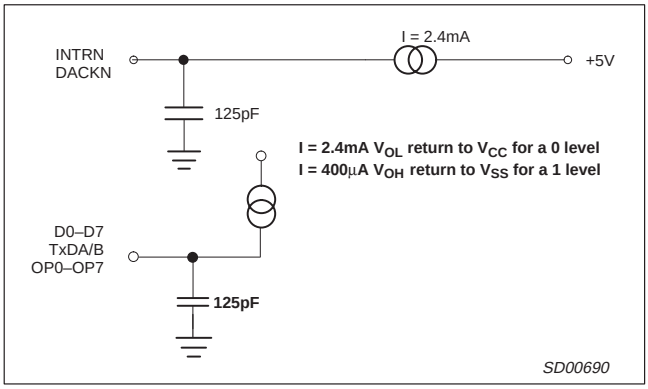
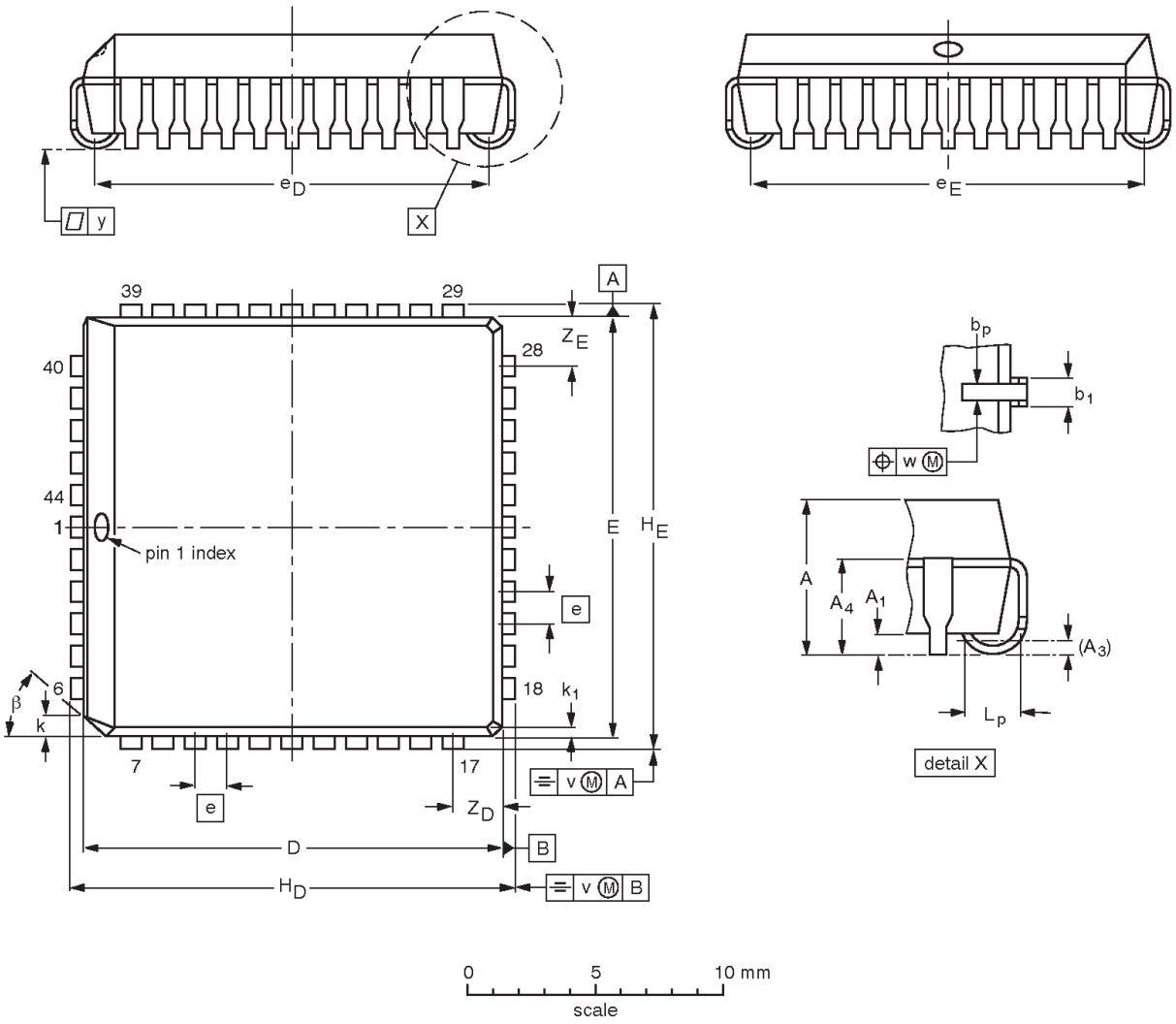


Figure 17. Test Conditions on Outputs

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

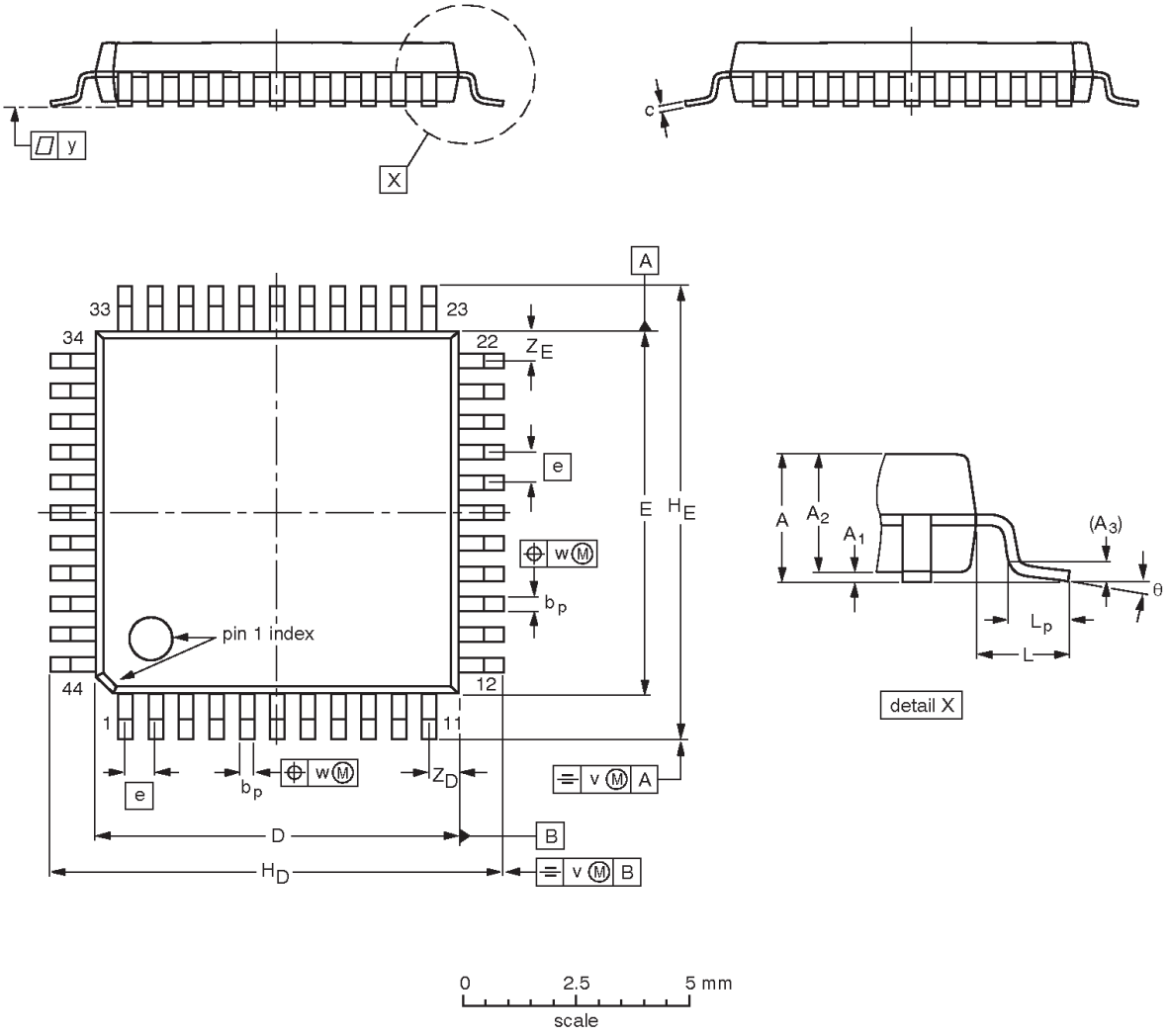
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~95-02-25~~ 97-12-16

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

3.3V–5.0V Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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